IN THE CLAIMS

1-8. (Canceled)

9. (Previously presented) A method of forming a trench isolation layer of a semiconductor device, comprising the steps of:

forming a trench-etching pattern for defining an active area on a substrate;

forming an isolation trench on the substrate using the trench-etching pattern as an etching mask;

forming a silicon nitride liner on inner walls of the trench;

forming a silicon oxide liner on inner sides of the silicon nitride liner;

performing heat treatment for hardening and densifying the silicon oxide liner;

filling the trench having the silicon oxide liner by depositing a first buried layer of silicon oxide;

partially etching the hardened and densified silicon oxide liner formed under the first buried layer of silicon oxide during recessing an upper surface of the first buried layer by etching; and

filling a remaining portion of the trench by depositing a second buried layer of silicon oxide on the first buried layer whose upper surface has been partially recessed by the etching.

10. (Previously presented) The method of claim 9, further comprising a step of forming a thermal oxide layer on the inner walls of the trench before the step of forming

the silicon nitride liner.

11. (Original) The method of claim 9, wherein the silicon oxide liner includes an HTO oxide layer, and the heat treatment is performed over about 1100°C for about 30 minutes to about 90 minutes.

12. (Previously presented) The method of claim 9, wherein the step of filling the trench with the first buried layer includes an SOG layer, and further comprising a curing step for changing the SOG layer into a silicon oxide layer before the step of etching the first buried layer.

13. (Previously presented) The method of claim 12, wherein the SOG layer includes a polysilazane series material, and the curing step is performed at a temperature of about 700°C to about 800° C for about 10 minutes to about 60 minutes.

14. (Previously presented) The method of claim 9, wherein the step of depositing the second buried layer includes performing HDP-CVD.

15. (Previously presented) The method of claim 9, further comprising the steps of:

exposing an upper part of the trench etching pattern by removing a portion of the second buried layer with a planarization etching; and

selectively removing the trench etching pattern.

16. (Previously presented) The method of claim 9, wherein the step of etching the first buried layer is processed by wet etching.

17. (Previously presented) The method of claim 9, wherein an etch rate of the silicon oxide liner is lower than an etch rate of the first buried layer of silicon oxide.